Amendments to the Claims

1. (previously presented) A feedback loop circuit apparatus for reducing DC offset in a communication channel, comprising:

a summer coupled to ~~summing node in~~ a receiver channel, wherein a receiver channel signal is coupled as an first input to said summer ~~summing node~~; and

an integrator ~~that has~~ comprising an input coupled to ~~a second node of~~ said receiver channel, wherein an output of said integrator is coupled as a second input to said summer ~~summing node~~;

wherein said integrator has a time constant that is variable according to at least one control signal to vary a frequency response of the integrator.

2. (original) The apparatus of claim 1, wherein the communication channel is a wireless local area network (WLAN) receiver channel.

3. (cancelled)

4. (currently amended) The apparatus of claim 1, ~~wherein~~ further comprising means for controlling said integrator frequency response ~~is controlled~~ to vary ~~the~~ a frequency response of the feedback loop circuit to a first frequency response, a second frequency response, and a third frequency response each having a corresponding lower 3 dB frequency, wherein said first frequency response has a relatively low lower 3 dB frequency, said second frequency response has a relatively medium lower 3 dB

frequency, and said third frequency response has a relatively greater lower 3 dB frequency.

5. (original) The apparatus of claim 1, wherein said integrator includes an amplifier, a capacitor, and a resistor arranged in an integrating amplifier configuration.

6. (original) The apparatus of claim 1, wherein said integrator includes an amplifier, a capacitor, and a variable resistor arranged in an integrating amplifier configuration.

7. (currently amended) The apparatus of claim 6, ~~wherein~~ further comprising means for varying said variable resistor ~~is varied~~ to alter the frequency response of said integrator.

8. (original) The apparatus of claim 7, wherein said variable resistor includes:

at least one resistor; and

at least one switch across said at least one resistor.

9. (currently amended) The apparatus of claim 7, wherein said variable resistor includes:

a first resistor;

a second resistor coupled in series with said first resistor;

a first switch coupled in parallel across said second resistor;

a third resistor coupled in series with said second resistor; and

a second switch coupled in parallel across said third resistor.

10. (currently amended) The apparatus of claim 9, wherein said first switch receives a first control signal, and said second switch receives a second control signal, and further comprising means for sequencing ~~wherein~~ said first and second control signals ~~are sequenced~~ in three consecutive time periods according to the following table:

	first control signal	second control signal
first time period	1	1
second time period	0	1
third time period	0	0

Cont.

11. (original) The apparatus of claim 10, wherein said third resistor has a larger resistance value than said second resistor, and wherein said second resistor has a larger resistance value than said first resistor.

12. (original) The apparatus of claim 10, wherein said first time period is within the range of 5 to 6 microseconds, and wherein said second time period is within the range of 55 to 128 microseconds.

13. (original) The apparatus of claim 1, wherein said integrator is configured in an inverting integrator configuration.

14. (currently amended) The apparatus of claim 1, further comprising:

at least one amplifier that couples said ~~second node~~ receiver channel to said input of said integrator.

15. (currently amended) The apparatus of claim 14, wherein said at least one amplifier is configured as a differential amplifier.

16. (original) The apparatus of claim 1, wherein said receiver channel signal is a radio frequency signal.

17. (original) The apparatus of claim 1, wherein said receiver channel signal is an intermediate frequency signal.

18-25. (Canceled)

26. (previously presented) A method for reducing DC offset in a communication channel, comprising the steps of:

(1) integrating an output signal available at a first node to generate an integrated signal;

(2) summing the integrated signal with a receiver channel signal at a second node, wherein the first node is downstream from the second node in a receiver channel; and

(3) varying a time constant associated with step (1) in response to at least one control signal to vary a frequency response of said integration.

27. (original) The method of claim 26, wherein the communication channel is a wireless local area network (WLAN) receiver channel.

28. (original) The method of claim 26, wherein step (1) includes the step of:

generating the integrated signal as an integrated and inverted version of the output signal.

29. (original) The method of claim 26, wherein step (1) is performed by an integrator circuit, wherein the integrator circuit includes an amplifier, a capacitor, and a resistor, the method further comprising the step of:

arranging the amplifier, capacitor, and resistor in an integrating amplifier configuration.

30. (cancelled)

31. (previously presented) The method of claim 29, wherein the integrator circuit includes an amplifier, a capacitor, and a variable resistor, the method further comprising the step of:

arranging the amplifier, capacitor, and variable resistor in an integrating amplifier configuration.

32. (previously presented) The method of claim 31, wherein step (3) comprises the step of:

varying the value of the variable resistor to alter the frequency response of the integrator circuit.

33. (currently amended) The method of claim [[32]] 31, further comprising the step of:

(i) configuring the variable resistor.

Cont.

34. (currently amended) The method of claim 33, wherein the variable resistor includes at least one resistor and at least one switch, step (i) comprising the step of:

coupling said at least one switch in parallel across said at least one resistor.

35. (currently amended) The method of claim 33, wherein the variable resistor includes a first resistor, a first switch, a second resistor, a second switch, and a third resistor, step (i) comprising the steps of:

coupling the first switch in parallel across the second resistor;

coupling the second resistor in series with the first resistor;

coupling the second switch in parallel across the third resistor; and

coupling the third resistor in series with the second resistor.

36. (currently amended) The method of claim 35, wherein the first switch receives a ffirst control signal and said second switch receives a second control signal, further comprising the step[[s]] of:

(I) ~~receiving a first control signal with the first switch;~~

~~(II) receiving a second control signal with the second switch; and~~

~~(III)~~—sequencing the first and second control signals according to the following table:

	first control signal	second control signal
first time period	1	1
second time period	0	1
third time period	0	0

Cont.

37. (currently amended) The method of claim 36, wherein step [[(III)]] (I) comprises the step of:

sequencing the first and second control signals, wherein the first time period is in the range of 4 to 6 microseconds, and wherein the second time period is in the range of 55 to 128 microseconds.

38. (original) The method of claim 36, further comprising the steps of:

receiving a data frame preamble during the first and second time periods; and

receiving a data portion of the data frame corresponding to the preamble during the third time period.

39. (original) The method of claim 26, wherein step (2) comprises the step of:

receiving the receiver channel signal, wherein the receiver channel signal is a radio frequency signal.

40. (original) The method of claim 26, wherein step (2) comprises the step of:

receiving the receiver channel signal, wherein the receiver channel signal is an intermediate frequency signal.

41-48. (Canceled)

49. (previously presented) A method for reducing DC offset in a communication channel, comprising the steps of:

(1) measuring a DC offset voltage present in an output signal at a first node, including the step of integrating the output signal available at the first node to generate an integrated signal that includes the DC offset voltage, wherein said integrating is performed by an integrator circuit;

(2) removing the measured DC offset voltage from a receiver channel signal at a second node, wherein the first node is downstream from the second node in a receiver channel; and

(3) varying a time constant of the integrator circuit in response to at least one control signal to vary a frequency response of the integrator circuit.

50. (cancelled)

51. (previously presented) The method of claim 49, wherein step (2) comprises the step of:

subtracting the integrated signal from the receiver channel signal at the second node.

52. (original) The method of claim 49, wherein the communication channel is a wireless local area network (WLAN) receiver channel.

53. (currently amended) A feedback loop circuit apparatus for reducing DC offset in a communication channel, comprising:

a ~~summing node in~~ summer coupled to a receiver channel, wherein a receiver channel signal is coupled as an first input to said summer ~~summing node~~; and

an integrator comprising ~~that has~~ an input coupled to ~~a second node of~~ said receiver channel, wherein an output of said integrator is coupled as a second input to said summer ~~summing node~~;

wherein said integrator includes an amplifier, a capacitor, and a variable resistor arranged in an integrating amplifier configuration;

wherein said variable resistor is varied to alter [[the]] a frequency response of said integrator;

wherein said variable resistor includes:

a first resistor,

a second resistor coupled in series with said first resistor,

a first switch coupled in parallel to ~~across~~ said second resistor,

a third resistor coupled in series with said second resistor, and

a second switch coupled in parallel to ~~across~~ said third resistor.

54. (currently amended) The apparatus of claim 53, wherein said first switch receives a first control signal, and said second switch receives a second control signal,

further comprising means for sequencing ~~wherein~~ said first and second control signals ~~are sequenced~~ in three consecutive time periods according to the following table:

	first control signal	second control signal
first time period	1	1
second time period	0	1
third time period	0	0

55. (currently amended) The apparatus of claim [[54]] 53, wherein said third resistor has a larger resistance value than said second resistor, and wherein said second resistor has a larger resistance value than said first resistor.

56. (previously presented) The apparatus of claim 54, wherein said first time period is within the range of 5 to 6 microseconds, and wherein said second time period is within the range of 55 to 128 microseconds.

57. (currently amended) A method for reducing DC offset in a communication channel, comprising the steps of:

(1) arranging an amplifier, capacitor, and variable resistor in an integrating amplifier configuration, wherein the variable resistor includes a first resistor, a first switch, a second resistor, a second switch, and a third resistor;

(2) configuring the variable resistor, including the steps of:

coupling the first switch in parallel across the second resistor,

coupling the second resistor in series with the first resistor,

coupling the second switch in parallel across the third resistor, and

coupling the third resistor in series with the second resistor;

(3) integrating an output signal available at a first node to generate an integrated signal, wherein said integrating is performed by an integrator circuit, wherein the integrator circuit includes the amplifier, capacitor, and variable resistor;

(4) summing the integrated signal with a receiver channel signal at a second node, wherein the first node is downstream from the second node in a receiver channel; and

(5) varying the frequency response of the integrator circuit in response to a control signal, including the step of varying the value of the variable resistor to alter the frequency response of the integrator circuit.

58. (currently amended) The method of claim 57, wherein the first switch receives a first control signal and the second switch receives a second control signal, further comprising the step[[s]] of:

(I) ~~receiving a first control signal with the first switch;~~

~~(II) receiving a second control signal with the second switch; and~~

~~(III)~~ sequencing the first and second control signals according to the following table:

	first control signal	second control signal
first time period	1	1

second time period	0	1
third time period	0	0

59. (currently amended) The method of claim 58, wherein step [[(III)]] (I) comprises the step of:

sequencing the first and second control signals, wherein the first time period is in the range of 4 to 6 microseconds, and wherein the second time period is in the range of 55 to 128 microseconds.

60. (previously presented) The method of claim 58, further comprising the steps of:

receiving a data frame preamble during the first and second time periods; and

receiving a data portion of the data frame corresponding to the preamble during the third time period.

61. (new) A communications system that includes a feedback loop circuit for reducing DC offset in a communication channel, comprising:

a summer coupled to a receiver channel, wherein a receiver channel signal is coupled as an first input to said summer; and

an integrator comprising an input coupled to said receiver channel, wherein an output of said integrator is coupled as a second input to said summer;

wherein said integrator has a time constant that is variable according to at least one control signal to vary a frequency response of the integrator.

62. (new) The system of claim 61, wherein the communication channel is a wireless local area network (WLAN) receiver channel.

63. (new) The system of claim 61, wherein said integrator frequency response is controlled to vary the frequency response of the feedback loop circuit to a first frequency response, a second frequency response, and a third frequency response each having a corresponding lower 3 dB frequency, wherein said first frequency response has a relatively low lower 3 dB frequency, said second frequency response has a relatively medium lower 3 dB frequency, and said third frequency response has a relatively greater lower 3 dB frequency.

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64. (new) The system of claim 61, wherein said integrator includes an amplifier, a capacitor, and a resistor arranged in an integrating amplifier configuration.

65. (new) The system of claim 61, wherein said integrator includes an amplifier, a capacitor, and a variable resistor arranged in an integrating amplifier configuration.

66. (new) The system of claim 65, wherein said variable resistor is varied to alter the frequency response of said integrator.

67. (new) The system of claim 66, wherein said variable resistor includes:

at least one resistor; and

at least one switch coupled in parallel across said at least one resistor.

68. (new) The system of claim 66, wherein said variable resistor includes:

a first resistor;

a second resistor coupled in series with said first resistor;

a first switch coupled in parallel across said second resistor;

a third resistor coupled in series with said second resistor; and

a second switch coupled in parallel across said third resistor.

69. (new) The system of claim 68, wherein said first switch receives a first control signal, and said second switch receives a second control signal, further comprising means for sequencing said first and second control signals in three consecutive time periods according to the following table:

	first control signal	second control signal
first time period	1	1
second time period	0	1
third time period	0	0

70. (new) The system of claim 69, wherein said third resistor has a larger resistance value than said second resistor, and wherein said second resistor has a larger resistance value than said first resistor.

71. (new) The system of claim 69, wherein said first time period is within the range of 5 to 6 microseconds, and wherein said second time period is within the range of 55 to 128 microseconds.

72. (new) The system of claim 61, wherein said integrator is configured in an inverting integrator configuration.

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73. (new) The system of claim 61, further comprising:

at least one amplifier that couples said second node to said input of said integrator.

74. (new) The system of claim 73, wherein said amplifier is configured as a differential amplifier.

75. (new) The system of claim 61, wherein said receiver channel signal is a radio frequency signal.

76. (new) The system of claim 61, wherein said receiver channel signal is an intermediate frequency signal.

77. (new) The apparatus of claim 1, wherein said summer is a node.

78. (new) The apparatus of claim 1, wherein said summer is a summing circuit.

79. (new) The apparatus of claim 53, wherein said summer is a node.

80. (new) The apparatus of claim 53, wherein said summer is a summing circuit.

81. (new) The system of claim 61, wherein said summer is a node.

82. (new) The system of claim 61, wherein said summer is a summing circuit.